Abstract of the Disclosure

A variable delay line includes a shift register responsive to coarse adjustment control and a fine adjustment control. The variable delay line can be used in a delay lock loop within an integrated circuit. The variable delay line receives coarse and fine adjustment controls from phase comparators within a phase detector. The coarse and fine adjustment controls cause a shift register associated with the delay element to shift varying amounts, thereby causing a varying amount of delay to be added or removed from the variable delay line. The shift register can be grouped into blocks, and the shift register can shift a block at a time in response to the coarse controls. The variable delay line can also include coarse delay cells associated with one shift register and fine delay cells associated with another shift register. One shift register adds or removes coarse delay cells in response to the coarse controls, the other shift register adds or removes fine delay cells in response to the fine controls.

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